Bruno BODIN

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General informations

Professional Experience

Since 2018 **Assistant Professor**, *Yale-NUS College*, Singapore.
2014-2018 **Research Associate**, *University of Edinburgh*, United Kingdom.
2011-2014 **Software Engineer**, *Kalray Company*, Orsay, France.
2010 **Research Engineer**, *LIP6*, Paris, France.

University Education

2010-2013 **Doctorate Degree (PhD)**, *Université Pierre & Marie Curie*, Paris, France.
2008-2010 **Master Degree – Computer Science**, *Université Pierre & Marie Curie*, Paris, France.

Research

Peer-reviewed Publications

[P1] Sam Nicholas Kouteili, Francesca Spagnuolo, Bruno Bodin. Strictly Periodic Scheduling of Cyclo-Static Dataflow Models. In International Conference on Embedded Computer Systems : Architectures, Modeling, and Simulation, (SAMOS XXI), Samos, Greece, 5-7 July, 2021

[P2] Bruno Bodin, Alix Munier-Kordon. Evaluation of the Exact Throughput of a Synchronous DataFlow Graph. Journal of Signal Processing Systems, 2021

[P3] Vanchinathan Venkataramani, Bruno Bodin, Aditi Kulkarni, Tulika Mitra, Li-Shiuan Peh. Time-predictable software-defined architecture with sdf-based compiler flow for 5G baseband processing. 45th International Conference on Acoustics, Speech, and Signal Processing (ICASSP), 2020

[P4] Mihai Bujanca, Paul-Adrian Gafton, Sajad Saeedi, Andrew Nisbet, Bruno Bodin, Michael F P OBoyle, Andrew J Davison, Paul H J Kelly, Graham Riley, Barry Lennox, Mikel Lujn, Steve Furber. SLAMBench 3.0: Systematic Automated Reproducible Evaluation of SLAM Systems for Robot Vision Challenges and Scene Understanding. International Conference on Robotics and Automation (ICRA'19), 2019

[P5] Kuba Kaszyk, Harry Wagstaff, Tom Spink, Björn Franke, Michael O'Boyle, Bruno Bodin, Henrik Uhrenholt. Full-System Simulation of Mobile CPU/GPU Platforms. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS'19), 2019

[P6] Michael Mendler, Joaquín Aguado, Bruno Bodin, Partha Roop, Reinhard von Hanxleden. Logic Meets Algebra: Compositional Timing Analysis for Synchronous Reactive Multithreading. Models, Mindsets, Meta: The What, the How, and the Why Not?, 2019

[P7] Cano Reyes, J., Yang, Y., Bodin, B., Nagarajan, V. and O'Boyle. Automatic Parameter Tuning of Motion Planning Algorithms. International Conference on Intelligent Robots and Systems (IROS'18), 2018

[P8] Saeedi, S. , Bodin, B. , Wagstaff, H. , Nisbet, A. , Nardi, L. , Mawer, J. , Melot, N. , Palomar, O. , Vespa, . E. , Spink, T. , Gorgovan, C. , Webb, A. , Clarkson, J. , Tomusk, E-A. , Debrunner, T. , Kaszyk, J. , Gonzalez-de-Aledo, P. , Rodchenko, A. , Riley, G. , Kotselidis, C. and 6 others. Navigating the Landscape for Real-time Localisation and Mapping for Robotics, Virtual and Augmented Reality. Proceedings of the IEEE, 2018

[P9] Bruno Bodin, Harry Wagstaff, Sajad Saeedi, Luigi Nardi, Emanuele Vespa, John Mawer, Andy Nisbet, Mikel Luján, Steve Furber, Andrew J. Davison, Paul H. J. Kelly, and Michael F. P. O'Boyle. SLAMBench2: Multi-Objective Head-to-Head Benchmarking. International Conference on

Robotics and Automation (ICRA'18), 2018

[P10] Philip Ginsbach, Toomas Remmelg, Michel Steuwer, Bruno Bodin, Christophe Dubach, and Michael F. P. O'Boyle. Automatic matching of legacy code to heterogeneous APIs: An idiomatic approach. International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS, 2018

[P11] Joaquin Aguado, Michael Mendler, Jiajie Wang, Partha Roop and Bruno Bodin. Compositional Timing-Aware Semantics for Synchronous Programming. Forum on specification & Design Languages (FDL'17), 2017

[P12] Jiajie Wang, Michael Mendler, Partha S. Roop and Bruno Bodin. Timing analysis of synchronous programs using WCRT Algebra: Scalability through abstraction. ACM Transactions on Embedded Computing Systems (TECS), 2017

[P13] Harry Wagstaff, Bruno Bodin, Tom Spink and Björn Franke. SimBench: A Portable Benchmarking Methodology for Full-System Simulators. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS'17), 2017

[P14] Sajad Saeedi, Luigi Nardi, Edward Johns, Bruno Bodin, Paul H. J. Kelly, and Andrew J. Davison. Application-oriented Design Space Exploration for SLAM Algorithms. International Conference on Robotics and Automation (ICRA'17), 2017

[P15] Bruno Bodin, Luigi Nardi, Paul HJ Kelly and Michael FP O'Boyle. Diplomat: Mapping of Multi-kernel Applications Using Static Dataflow Abstraction. IEEE 24th International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS'16), 2016

[P16] Michael Mendler, Partha S. Roop and Bruno Bodin. A Novel WCET semantics of Synchronous Programs. 14th International Conference on Formal Modeling and Analysis of Timed Systems (FORMATS'16), 2016

[P17] Bruno Bodin, Luigi Nardi, M Zeeshan Zia, Govind Sreekar Shenoy, Murali Emani, John Mawer, Christos Kotselidis, Andy Nisbet, Mikel Luján, Björn Franke, Paul Kelly and Michael O'Boyle. Design exploration across domain and implementation in dense 3D scene understanding. 25th International Conference on Parallel Architectures and Compilation Techniques (PACT'16), 2016

[P18] M Zeeshan Zia, Luigi Nardi, Andrew Jack, Emanuele Vespa, Bruno Bodin, Paul HJ Kelly and Andrew J Davison. Comparative Design Space Exploration of Dense and Semi-Dense SLAM. In International Conference on Robotics and Automation (ICRA'16), 2016

[P19] Bruno Bodin, Alix Munier-kordon, and Benoît Dupont de Dinechin. Optimal and fast throughput evaluation of CSDF. In Design Automation Conference (DAC'16), pages 1-6, Austin, TX, USA, 2016

[P20] Luigi Nardi, Bruno Bodin, M Zeeshan Zia, John Mawer, Andy Nisbet, Paul HJ Kelly, Andrew J Davison, Mikel Luján, Michael FP O'Boyle, Graham Riley, Nigel Topham, Steve Furber. Introducing SLAMBench, a performance and accuracy benchmarking methodology for SLAM. In International Conference on Robotics and Automation (ICRA'15), pages 5783–5790, 2015

[P21] Bruno Bodin, Youen Lesparre, Jean-Marc Delosme, Alix Munier-Kordon. Fast and efficient dataflow graph generation. In Proceedings of the 17th International Workshop on Software and Compilers for Embedded Systems (SCOPES'14) pages 40-49, 2014

[P22] Pascal Aubry, Pierre-Edouard Beaucamps, Frédéric Blanc, Bruno Bodin, Sergiu Carpov, Loïc Cudennec, Vincent David, Philippe Dore, Paul Dubrulle, Benoît Dupont de Dinechin, François Galea, Thierry Goubier, Michel Harrand, Samuel Jones, Jean-Denis Lesage, Stéphane Louise, Nicolas Morey Chaisemartin, Thanh Hai Nguyen, Xavier Raynaud and Renaud Sirdey. Extended Cyclostatic Dataflow Program Compilation and Execution for an Integrated Manycore Processor. In Proceedings of the International Conference on Computational Science (ICCS 2013), pages 1624-1633, Barcelona, Spain, 5-7 June, 2013

[P23] Mohamed Benazouz, Alix Munier-Kordon, Thomas Hujsa, et Bruno Bodin. Liveness Evaluation of a Cyclo-Static DataFlow Graph. In Design Automation Conference (DAC'13), pages 3:1—3:7, Austin, TX, USA, 2013

[P24] Bruno Bodin, Alix Munier-kordon, and Benoît Dupont de Dinechin. Periodic Schedules for Cyclo-Static Dataflow. ESTIMedia'13, pages 105–114, 2013

[P25] Bruno Bodin, Alix Munier-Kordon, and Benoît Dupont de Dinechin. K-Periodic Schedules for Evaluating the Maximum Throughput of a Synchronous Dataflow Graph. In International Conference on Embedded Computer Systems : Architectures, Modeling, and Simulation, (SAMOS XII), pages 152–159, Samos, Greece, 16-19 July, 2012

Conference Abstracts

[P26] Martin Kristien, Bruno Bodin, Michel Steuwer, Christophe Dubach. High-Level Synthesis of Functional Patterns with Lift. 6th ACM SIGPLAN International Workshop on Libraries, Languages, and Compilers for Array Programming, 2019

[P27] M. Bujanca, P. Grafton, S. Saeedi, A. Nisbet, B. Bodin, M. F.P. O'Boyle, A. J. Davison, P. H.J. Kelly, G. Riley, B. Lennox, M. Luján, S. Furber. SLAMBench3.0: Systematic Automated Reproducible Evaluation of SLAM Systems for Robot Vision Challenges and Scene Understanding. In DGB-ICRA, 2019

[P28] Bruno Bodin, Luigi Nardi, Harry Wagstaff, Paul H. J. Kelly and Michael O'Boyle. Algorithmic Performance-Accuracy Trade-off in 3D Vision Applications. In ISPASS, 2018

[P29] Michael Mendler, Partha S. Roop and Bruno Bodin. WCET semantics of Synchronous Program. In SYNCHRON, 2016

[P30] Michael Mendler, Bruno Bodin, Partha S. Roop and Jia Jie Wang. Worst-case Reaction Time for Synchronous Programs – Studying the Tick Alignment Problem. In SYNCHRON, 2014

[P31] Michael Mendler, Bruno Bodin, Partha S. Roop and Jia Jie Wang. The WCRT analysis of synchronous programs: Studying the tick alignment problem. In REPP, 2014

[P32] Bruno Bodin, Benoît Dupont de Dinechin, Alix Munier-Kordon. Evaluation du débit maximum d'un Synchronous DataFlow. In ROADEF, 2013

Professional services

Organizing Committee

2021 **Artefact Evaluation Chair**, *Compiler Construction (CC)*, USA.

2020 **Artefact Evaluation Co-chair**, *Compiler Construction (CC)*, USA.

2019 **Artefact Evaluation Co-chair**, *Languages, Compilers, Tools and Theory of Embedded Systems (LCTES)*, USA.

2019 **Co-organiser**, *Dataset Generation and Benchmarking of SLAM Algorithms for Robotics and VR/AR at ICRA'19*, Montreal,Canada.

2018 **Co-organiser**, *GenSim tutorial at ISPASS'18*, UK.

2017 **Tutorial chair**, *15th International Conference on High Performance Computing & Simulation (HPCS)*, Italy.

2016 **Co-organiser**, *SLAMBench tutorial at FPL'16*, Switzerland.

2016 **Co-organiser**, *ASR-MOV workshop at CGO'16*, Barcelona.

2011-2013 **Web Chair**, *French research group GDR-ROElec*, France.

Technical Program Committee

2020 ACM Int. Symposium on Performance Analysis of Systems and Software: **ISPASS** (PC Member)

2019 ACM Int. Workshop on Code Optimisation for Multi and Many-Cores: **COSMIC** (PC Member)

2018 ACM Int. Conference on Parallel Architectures and Compilation Techniques: **PACT** (PC Member)

2017 ACM Int. Workshop on Code Optimisation for Multi and Many-Cores: **COSMIC** (PC Member)

External reviews

2021 Springer Journal of Signal Processing Systems (**JSPS**)

2020 Springer Journal of Signal Processing Systems (**JSPS**), ACM Transactions on Architecture and Code Optimization (**TACO**), Springer Robotics and Autonomous Systems (**ROBOT**), ACM Transactions on Embedded Computing Systems (**TECS**), ACM/EDAC/IEEE Design and Automation Conference (**DAC**), IEEE International Conference on Robotics and Automation (**ICRA**)

2019 ACM Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), IEEE Computer Architecture Letters (**CAL**), ACM/EDAC/IEEE Design and Automation Conference (**DAC**), IEEE/RSJ Int. Conference on Intelligent Robots and Systems (**IROS**), IEEE Transactions on Very Large Scale Integration (**VLSI**)

2018 IEEE Transactions on Computing (**TC**), IEEE Computer Architecture Letters (**CAL**), ACM Compiler Construction (**CC**), ACM Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)

2017 IEEE Embedded System Letters (**ESL**), ACM SIGBED International Conference on Embedded Software (**EMSOFT**), ACM Transactions on Embedded Computing Systems (**TECS**), ACM SIGPLAN/SIGBED Conference on Languages, Compilers, Tools and Theory for Embedded Systems (**LCTES**)

2016 Wiley Concurrency and Computation: Practice and Experience(**CPE**), IEEE Embedded System Letters (**ESL**), ACM Transactions on Architecture and Code Optimization (**TACO**), ACM/IEEE International Symposium on Code Generation and Optimization (**CGO**), ACM SIGPLAN/SIGBED Conference on Languages, Compilers, Tools and Theory for Embedded Systems (**LCTES**)

2015 ACM Transactions on Architecture and Code Optimization (**TACO**), ACM/IEEE International Symposium on Code Generation and Optimization (**CGO**), ACM International Conference on Parallel Architectures and Compilation Techniques (**PACT**)

2014 ACM/EDAC/IEEE Design and Automation Conference (**DAC**), IEEE International Conference on Embedded Computer Systems: Architecture MOdeling and Simulation (**SAMOS**), ACM Transactions on Embedded Computing Systems (**TECS**), ACM/IEEE International Symposium on Code Generation and Optimization (**CGO**)

2013 IEEE International Symposium on Rapid System Prototyping (**RSP**)

Membership of Professional Bodies

2017-2020 Member of the Institute of Electrical and Electronics Engineers (IEEE)

2014-2020 Member of the Association for Computing Machinery (ACM)

2014-2016 Member of the British Machine Vision Association (BMVA)

2012-2014 Member of the French Operational Research community (ROADEF)